D3.2 Design tools including power systems models, chosen architectures, protection systems and converters models and simulation procedures

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Summary

1 DC Systems - Protection Plan - Design Intent

Abbreviations and designations

Naming	Equipment	Description
AC	Alternating Current	
AVR	Automatic Voltage Regulator	
CB	Circuit Breaker	
DC	Direct Current	
DnV	Classification Society	Det norske Veritas
DE	Diesel Generator Engine	
ESS	Energy Storage System	
Fn	Nominal Frequency(Hz)	
G	Alternator	
GB	Generator Breaker	Breaker in main switchboard
GC	Generator converter	Located in the DC SWB
In	Nominal Current(A)	
LV	Low Voltage	
MP	Main Propulsion	
ePMS	Energy Power Management System	SeaQ Control
Pn	Nominal Power(kW)	
PS	Port Side	
SSB	Sold-state based bus-tie breaker	Bus-tie between the different sections.
STB	Star Board	
SWB	Switchboard (Main)	SeaQ Power
SRtP	Safe Return to Port	Class notation
Un	Nominal Voltage(V)	
VSC	Voltage Source Converter	
>	Greater than	
<	Less than	

Regarding the definitions in table, alternative names like GCB (instead of GB) and SSCB (instead of SSB) can be also considered, as more utilized in technical literature. Anyway, the explained definition in table are still valid.

1.1 Descriptions

This document offers insights into the approach for protection coordination and serves as an informational resource. It includes details on the protection settings and philosophy for the DC SWB and corresponding sources, complemented by logic functions. The focus is on the intent for selectivity and the division of redundancy.

1.1.1 Selectivity

Ensuring coordination between protection devices enabled the immediate upstream breaker to respond effectively. Selectivity is designed to minimize interruptions within the DC SWB, focusing on isolating the affected area while maintaining overall system stability.

1.1.2 Redundancy group split

To achieve a safe return to port (SRtP) with a closed bus-tie system, it is necessary to ride through the duration needed for fault clearing. The intention is to split the bus-tie before clearing the fault, thereby ensuring uptime in the healthy groups, and enhancing overall system resilience.

1.2 Protection devices

This chapter will provide a description of the various protection devices used in the DC SWB, outlining their functions, characteristics, and roles in ensuring the safety of the system.

1.2.1 Generator converter

The generator converter cabinet is equipped with AC breaker for isolation. Furthermore, the generator converter features monitoring for under/over voltage, over current, and imbalance. In response to these conditions, it takes actions tripping the AC breaker, stopping modulation, and demagnetizing the generator.

For internal protection of the synchronous generator, short circuit relay type is utilized with current transformers installed on the star side.

1.2.2 Power modules

Protection and selectivity within the various DC SWB sections is managed by solid-state based breakers in each power module, which immediately interrupt an upstream short-circuit.

1.2.3 Solid-state based bus-tie breaker

The solid-state based bus-tie breaker (SSB) is a fast DC current interruption device designed to detect and cut off an outgoing short-circuit current. Its main task is to isolate the faulty DC-link from the healthy DC-link. The SSB will isolate the faulty part of the system within 10 microseconds. The SSB is equipped with mechanical disconnectors to ensure safe isolation of voltage after the IGBTs have cut the current. Should a fault occur in one of the breakers, it will lead to the opening of the other breaker.

The SSB is monitored and controlled by the ePMS.

1.2.4 Energy storage system

For the various battery systems, semiconductor fuses are installed on both the battery and the DC/DC converter to provide short-circuit protection.

1.2.5 Energy power management system

The ePMS have load control and power limitation of the different inverter units. Load control is provided for dynamic consumers like thrusters and propulsion inverters, to avoid overload on the generators. In addition, the ePMS will have interface towards the diesel engine control system and stop down if requested.

1.3 Protection plan

1.3.1 Protections

DESCRIPTION	SETTING (%)	DELAY (s)	TRIP	PROT.MOD	INHIBITS	COMMENTS
G Short circuit protection	150% In	instant	GB	GC		Alarm, Trip GB, De-magnetize generator
G Over-current protection	115% In	instant	GB	GC		Alarm, power limitation
G Over-voltage	106% Un	500 ms	GB	GC		Alarm, Trip GB, De-magnetize generator
G Over-frequency on AC side	105% Fn	1 s	GB	GC		Alarm, Trip GB, De-magnetize generator
G Current and voltage imbalance	10% Δ	5 s	GB	GC		Alarm, Trip GB, De-magnetize generator
G Internal Short-circuit protection	150% In	500 ms	GB	GC/RMC-111D		Alarm, Trip GB, De-magnetize generator
G Loss of sensing	Potential free relay	0	GB	AVR		AVR to open generator breaker
B Over-current 1	150% In	10	SSB	SSB		Alarm, trip SSB
B Over-current 2	170% In	instant	SSB	SSB		Alarm, trip SSB
E Overload	115% In	instant	BC	BC		Alarm, trip DC/DC
Earth fault monitoring						Alarm

SETTING AND DELAY CAN BE ADJUSTED

2 Short-circuit estimation of components

Short-circuit estimation for DC systems is a complex task for several reasons. Indeed, since the use of DC technology in power systems in general is of recent introduction, there is a lack of well-established standards for short-circuit calculation, as in conventional AC systems.

The main issues in DC short-circuit can be summarized as follows:

- Lack of zero-crossing of the current due to unidirectionality nature of the DC systems, resulting in more challenging circuit breakers operation.
- Integration of innovative technologies for energy storage systems (ESS).
- The presence of power converters interfaces between the ESSs and the main DC-bus, which implement internal protection logic to safeguard IGBTs from currents higher than the nominal value.
- The presence of capacitors in the DC-bus for voltage ripple attenuation and stability of the overall system, which lead to a high and very rapid current discharge in case of fault in the DC-bus.
- Selectivity and choice of the proper protection device can be challenging, due to the very steep rise time of the fault current.

The estimation of the short-circuit contribution of the different types of energy storage systems that will be integrated in the shipboard power system (SPS) is of paramount importance to its design process. Indeed, with a proper estimation of the short-circuit behavior of these components, it is possible to effectively size all the protection components, and the other components of a SPS, such as cables, busbars, and so on.

The philosophy used for the estimation of short-circuit behavior is to focus on the maximum and minimum short-circuit cases. The former is useful to determine the short-circuit let-through energy, allowing proper sizing of components. The latter is useful for the protection scheme design and tuning.

To characterize effectively the short-circuit behavior of the ESSs together with the dedicated converter interface in various conditions, the estimation of the short-circuit profile of the ESSs will be carried considering each source individually in the simulation environment, splitting the SPS into the minimum sets of components, which are the ESSs, together with the dedicated converter interface, the output filter capacitor, and an equivalent load.

A parametric study has been considered to explore the variation in short-circuit behavior of the ESSs when some key parameters are varied across a feasible interval.

To this extent, to perform the short-circuit calculations, Matlab/Simulink software has been used, employing the SimScape SimPowerSystem library.

Moreover, to verify the results of the simulations, an approach based on the analysis of equivalent RLC circuit of the fault is considered.

In the next subsections, the models for the batteries, supercapacitors and supermagnetic energy storage system (SMES) will be presented, which are based on data provided by the manufacturers. Then the converter used for interfacing the ESSs to the main DC-bus will be considered, together with the model of the DC-bus capacitor and the load. After that, the analytic approach based on the analysis of an equivalent RLC circuit of the fault is presented. Lastly, the simulation results will be presented.

2.1 Modeling of energy storage system and integration in simulation tool

In order to estimate the detailed short-circuit behavior of the ESSs together with their converter, Matlab/Simulink models of components have been developed, considering the data of ESSs from technology supplier, the converter and control models, and the model of the components such as the capacitor and the load. As an example, in Figure 1 the Simulink model for short-circuit estimation of the battery case is showed.

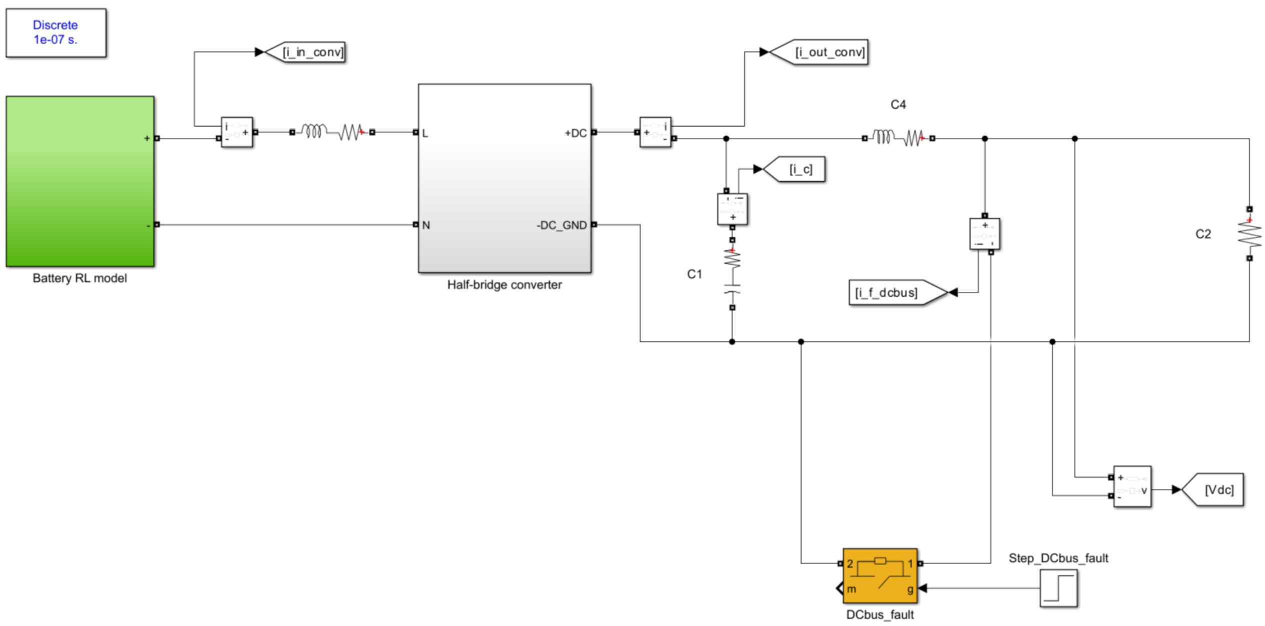

FIGURE 1: SIMULINK MODEL FOR SHORT-CIRCUIT ESTIMATION

2.1.1 Battery model

The battery models have been developed based on datasheet of Corvus Orca Energy batteries provided by Vard, which are reported in Table 1.

From these data, the model that has been developed is an ideal voltage source in series with an RL branch, which has been implemented in Simulink as in Figure 2.

Among all data, those that have been useful for the definition of the battery model are:

- Number of packs N_{packs}
- Maximum voltage ${V_b}^{max}$
- Minimum voltage ${V_b}^{min}$
- Short-circuit maximum current at beginning of life (BoL) I_{sc}^{max}
- Time constant of short-circuit current at BoL τ_{BoL}
- Short-circuit minimum current at end of life (EoL) I_{sc}^{min}
- Time constant of short-circuit current at EoL τ_{EoL}

TABLE 1: DATA FOR BATTERY

Number of packs	12, 6 FWD and 6 AFT
Total Dry Mass(+-15kg/pack, incl rack)	17 916 kg
Estimated lifetime	10 years
Data of one battery pack of type Corvus Orca	
Max voltage	1000 VDC
Min voltage	720 VDC
Energy	113 kWh
Capacity	128 Ah
C-Rate - Peak (Discharge / Charge)	up to 3C / up to 3C
C-Rate - Continuous (Discharge / Charge)	Project specific: 0.9C / 1.8C
Maximum current	500A
Short Circuit capacity	Max (BoL): current: 14,9 kA L/R: 0,16 ms
	Min (EoL): current: 6,4 kA L/R: 0,10 ms
Battery Cell Chemistry	Lithium ion NMC / graphite
Max Gravimetric Density - Pack	77 Wh/kg | 13 kg/kWh
Max Volumetric Density - Pack	88 Wh/l
Pack Configuration	Vertical
Pack footprint	865 mmL x 737 mmD
Pack height	2077 mmH
Pack weight	1493 kg
Safety Specifications:	
Thermal Runaway Anti-Propagation	Passive cell-level thermal runaway isolation with exhaust gas system
Fire Suppression	Per SOLAS, class and Corvus recommendation
Disconnect Circuit	Hardware-based fail-safe for over-temperature, over-voltage and under-voltage
Short Circuit Protection	Fuses included on pack level
Emergency Stop Circuit	Hard-wired
Ground Fault Detection	Integrated
Disconnect Switchgear Rating	Full load
General Specifications:	
Class Compliance	DNV , Lloyds Register, Bureau Veritas, ABS, RINA
Type Approval	DNV , Bureau Veritas, ABS, RINA
Ingress Protection	System: IP44
Cooling	Forced Air
Vibration and shock	UNT38.3, DNVGL-CG-0339 Class A, IEC 60068-2-6
EMC	DNVGL-CG-0339 Class A

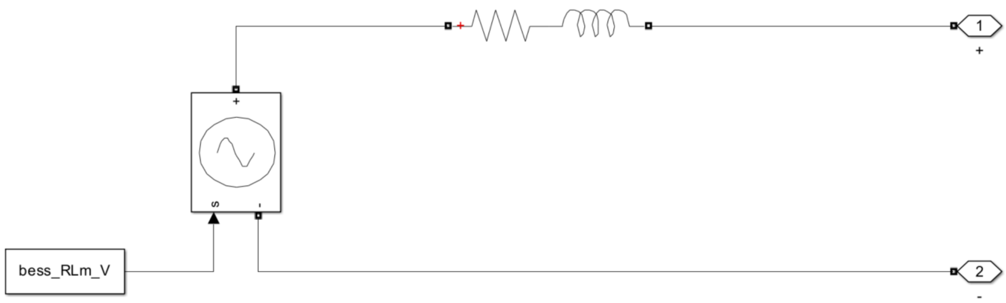

FIGURE 2: BATTERY MODEL

2.1.1.1 Battery parameters for maximum short-circuit estimation

For the maximum short-circuit estimation, the battery voltage considered is the fully charged voltage:

$$V_b = V_b{}^{max}$$

The battery parameters for the maximum short-circuit condition are referred to the BoL, thus for the resistance parameter at BoL:

$$R_{BoL} = \frac{1}{N_{packs}} \frac{V_b{}^{max}}{I_{sc}^{max}}$$

While the inductance parameter at BoL is derived from the resistance and the time constant of the short-circuit:

$$L_{BoL} = R_{BoL} \cdot \tau_{BoL}$$

2.1.1.2 Battery parameters for minimum short-circuit estimation

For the minimum short-circuit estimation, the battery voltage considered is the minimum voltage:

$$V_b = V_b{}^{min}$$

The resistance parameter at EoL can be derived as follows:

$$R_{EoL} = \frac{1}{N_{packs}} \frac{V_b{}^{min}}{I_{sc}^{min}}$$

While the inductance at EoL is obtained, as for the maximum short-circuit model, as follows:

$$L_{EoL} = R_{EoL} \cdot \tau_{EoL}$$

2.1.2 Supercapacitor model

The supercapacitor model has been developed based on the data provided by Skeleton, which are listed in Table 2.

TABLE 2: SUPERCAPACITOR DATA

Supercap module data	
Module configuration	5s14p
Rated voltage [V]	162
Rated capacitance [F]	62
Supercapacitor system data	
Number of modules per cabinet	10
Number of cabinets	7
Maximum voltage [V]	810
Minimum voltage [V]	650
Rated equivalent capacitance [F]	176
Rated equivalent series resistance [mΩ]	5

From these data, the model that has been developed is a RC branch, which has been implemented in Simulink as in Figure 3.

Among those data, those that have been useful for the definition of the models are:

- Maximum voltage V_{SC}^{max}
- Minimum voltage V_{SC}^{min}
- Rated equivalent capacitance C_{SC}
- Rated equivalent series capacitance $R_{SC,ESR}^{rated}$

FIGURE 3: SUPERCAPACITOR MODEL

2.1.2.1 Supercapacitor parameters for maximum short-circuit estimation

For the maximum short-circuit estimation, the supercapacitor voltage considered is the maximum operating voltage:

$$V_{SC}(0) = V_{SC}^{max}$$

The supercapacitor parameters for the maximum short-circuit condition are referred to the BoL, thus for the equivalent capacitance of the supercapacitor system:

$$C_{sc}^{BoL} = C_{sc}^{rated}$$

While for the equivalent series resistance (ESR):

$$R_{esr}^{BoL} = R_{esr}^{rated}$$

2.1.2.2 Supercapacitor parameters for minimum short-circuit estimation

For the minimum short-circuit estimation, the supercapacitor voltage considered is the minimum operating voltage:

$$V_{SC}(0) = V_{SC}^{min}$$

The RC model parameters are considered at the EoL. For the equivalent capacitance at the EoL it is considered a derating of the rated capacitance, as follows:

$$C_{sc}^{EoL} = 0.8 \cdot C_{sc}^{rated}$$

For the ESR at the EoL, the following increment of the rated ESR is considered, as follows:

$$R_{esr}^{EoL} = 2 \cdot R_{esr}^{rated}$$

2.1.3 Super magnetic energy storage system model

Differently the others ESSs, which behave as voltage sources, the SMES behaves as a current source, which provides a fixed current, depending on its State of Charge (SOC).

As for the other ESSs, two models of the SMES are presented, one for the maximum short-circuit estimation, and the other for the minimum short-circuit estimation.

The data needed for the realization of the SMES model are provided by ASG and are listed in Table 3.

TABLE 3: SMES DATA

Parameter	Value
Inner radius (mm)	300
Height (mm)	1200.6
Number of layers	10
Number of turns per layer	522
Cable length (km)	10.1
DC bus voltage (V)	750
Maximum power (kW)	200
Minimum current (A)	266.6
Maximum current (A)	467
Field on conductor (at Imax) (T)	1.63
I/Ic ratio (at Imax)	0.6
Inductance (H)	6.8
Total energy (at Imax) (kJ)	741
Deliverable energy (kJ)	500.4
Damping resistance (Ω)	2.14
Maximum adiabatic temperature of hot spot (°C)	95.6
maximum Current derivative (A/s)	110.3

Based on the data provided, the SMES is then modeled as an inductance, based on the following parameters:

- Coil inductance L_{smes}
- Maximum current I_{smes}^{max}
- Minimum current I_{smes}^{min}
- Nominal power P_{smes}
- Maximum current derivative $\left.\frac{\Delta I_{smes}}{\Delta t}\right|_{max}$

SMES quench protection have been considered in the realization of the model [8], which is shown in Figure 4 and Figure 5. The quench protection is composed by a set of switches and a damping resistor circuit. In normal conditions, the quench protection is inactive. In case of SMES quenching, the protection activates and the SMES current is redirected to a damping circuit, where the energy of the SMES is dissipated.

The quench protection is a protection scheme internal to the SMES, which can disconnect the SMES from the main circuit in case the following conditions occurs:

- $I_{smes} > I_{smes}^{max}$
- $\frac{di_{smes}}{dt} > \left.\frac{\Delta I_{smes}}{\Delta t}\right|_{max}$

In case the SMES variables exceed those thresholds, the quenching protection trigger the opening of the switch K2, and the closing of the switch K1, safely dissipating the SMES current in the damping resistance. The current derivative has been computed utilizing a filtered derivative, with a filter time constant of 5 ms.

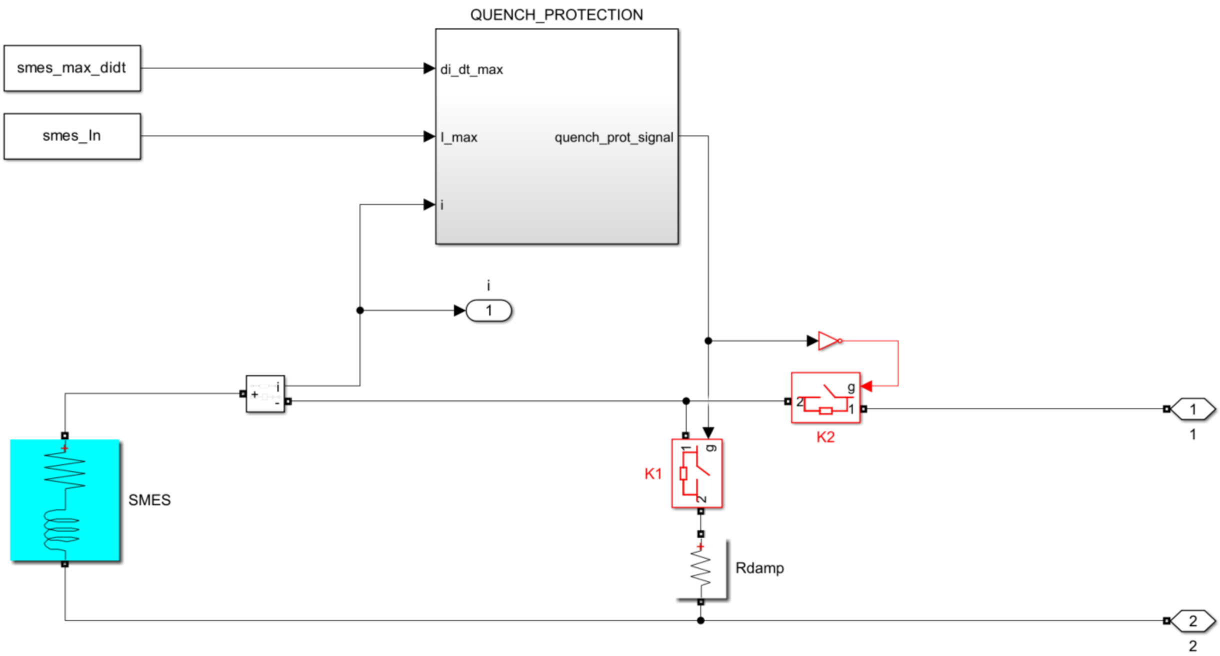

FIGURE 4: SMES MODEL

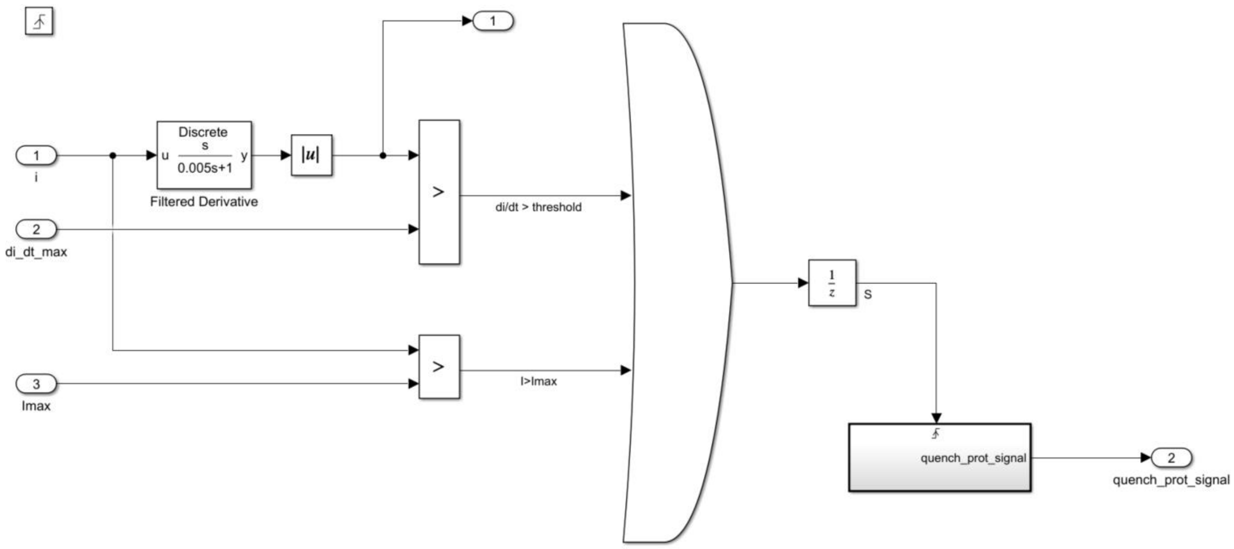

FIGURE 5: QUENCH PROTECTION

2.1.3.1 Super magnetic energy storage system model for maximum short-circuit estimation

The model is composed by the SMES equivalent inductance and the quench protection damping circuit. The initial current of the SMES is set to the maximum value of SMES current, therefore:

$$I_{smes}(0) = I_{smes}^{max}$$

2.1.3.2 Super magnetic energy storage system model for minimum short-circuit estimation

The model is composed by the SMES equivalent inductance and the quench protection damping circuit. The initial current of the SMES is set to 10% of the maximum SMES current, therefore:

$$I_{smes}(0) = 1.10 \cdot I_{smes}^{min}$$

2.1.4 Power converter interfaces for Energy storage systems

The models of the converters and control system that have been used for short-circuit estimation have been provided as Matlab/Simulink models by University of Birmingham (UoB).

The half bridge converter is the converter used for interfacing the battery and the supercapacitor to the DC-bus, whereas the full bridge converter is the converter used for interfacing the SMES to the DC-bus. These converters have both the function of controlling the power flow between the ESS and the DC-bus, and to match the voltage levels of these two components of the SPS.

The half-bridge converters used for the battery and the supercapacitor implement an internal current controller, which is composed by a standard PI controller, that generates the duty cycle reference to the PWM block, based on the error between a current reference and a measured current reference. The model of the converter and the control are shown in Figure 6.

The full-bridge converter used for the SMES implements a DC-bus proportional voltage controller, which generates a power reference signal. Then, the power reference signal is divided by the SMES measured current, obtaining the SMES reference voltage. An internal SMES voltage controller is then implemented, which generates the reference signal for the PWM, needed for supplying the request power from the external DC-bus voltage controller. The model of the converter and the control are shown in Figure 7.

The original models did not implement the IGBTs internal protection. Therefore, in order to simulate a more accurate behaviour of the converter in terms of fault, a simple model for IGBT protection have been developed.

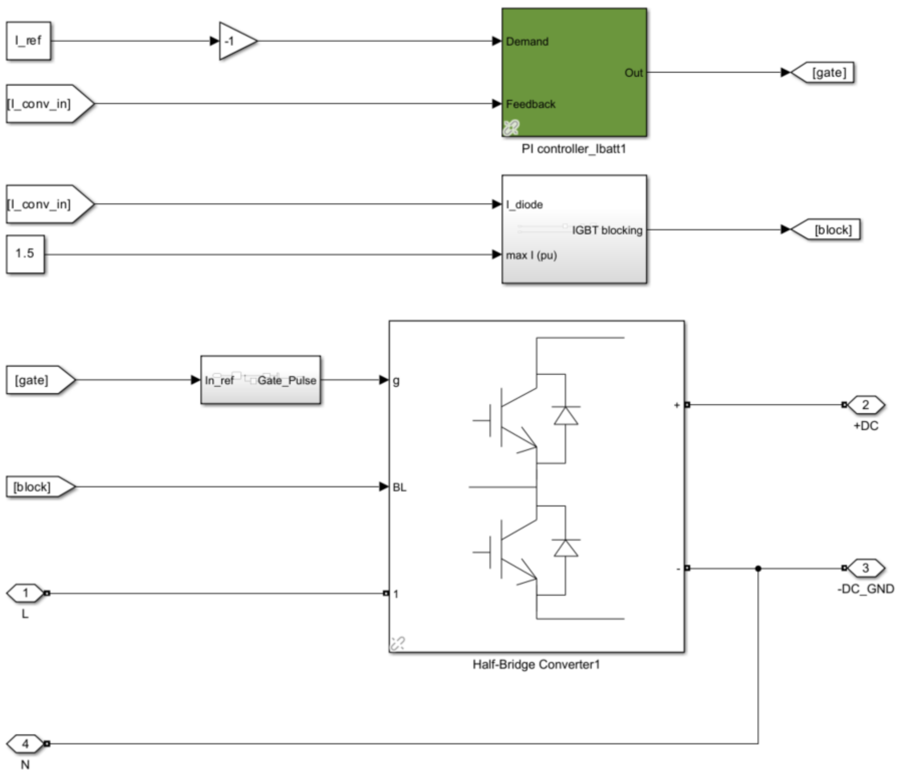

FIGURE 6: HALF-BRIDGE CONVERTER AND CURRENT CONTROLLER

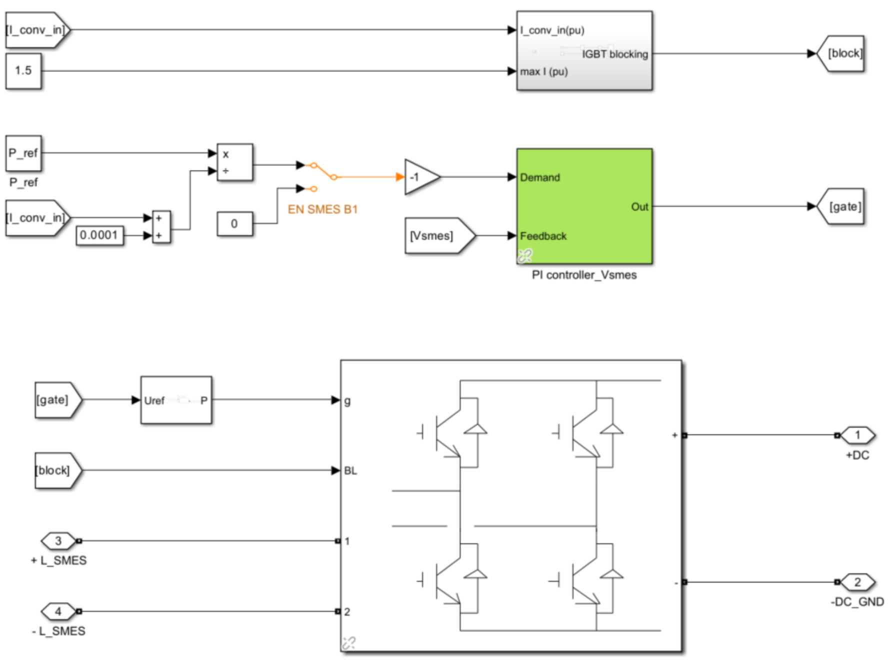

FIGURE 7: FULL-BRIDGE CONVERTER AND VOLTAGE CONTROLLER

The blocking scheme, shown in Figure 8 compares the input current of the converter with a selected threshold, which has been set to 1.5 times the nominal input current of the converter. Therefore, in case of a fault, when the current exceeds the specified threshold, the blocking scheme acts by turning off all the IGBTs of the converter.

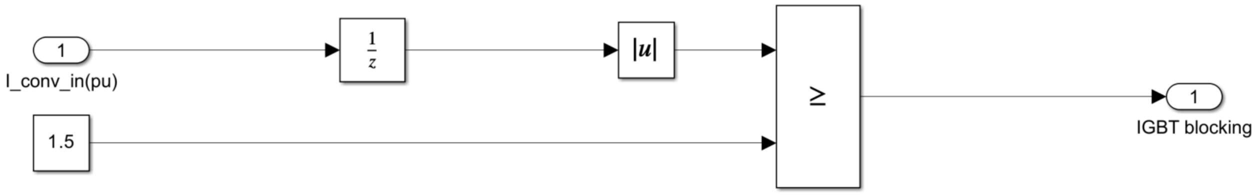

FIGURE 8: IGBT BLOCKING SCHEME

It must be noted that the two converter topologies employed for the interfacing of the ESSs to the DC-bus do not have fault-blocking capabilities, since the fault current can freely flow through the freewheeling diodes, which cannot be shut down.

2.1.5 DC-bus capacitor

The DC-bus capacitor is employed in DC microgrids for reduction of voltage ripple, and for enhancing stability of operations.

The DC-bus capacitor has been modeled as an RC terminal, where C is the nominal capacitance of the capacitor, and R is the equivalent series resistance (ESR) of the capacitor.

2.1.6 Considerations on the simulation environment

The simulation environment is Matlab/Simulink. The model is using components from the SimPowerSystem library, and all the components are discretized, to employ the fixed step discrete solver. The step size considered for the simulations is set to 100 ns.

2.1.7 Analytical estimation of short-circuit at the DC-bus

To offer a comparison of the simulation results with existing techniques, the analytic estimation of the short-circuit at the DC-bus is considered. The calculation procedure is presented in [1]. In this work, the power converter considered is a VSC, which is used to interface an AC source with the DC-bus. However, due to the presence of the dc-bus capacitor at the converter output, the initial capacitor discharge phase is shared among all type of converters that present an output capacitor [2], as for the half-bridge and full bridge converters considered in this work. Therefore, since the converter response is largely dominated by the initial capacitor response, it is possible to approximate the fault current with the capacitor current. This will be useful to ensure the correctness of the short-circuit data obtained from simulations.

In case of short-circuit at the DC-bus, the fault current will flow across the busbars, which present an inductive and resistive behavior. Therefore, this behavior can be modeled with an RL branch.

The resulting equivalent RLC circuit for the capacitor discharge phase is showed inFigure 9. This circuit model is valid starting from the short-circuit event, until the capacitor voltage drops to zero.

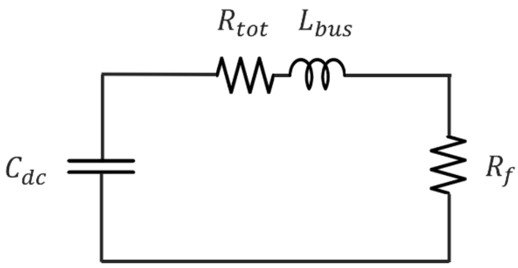

FIGURE 9: RLC EQUIVALENT CIRCUIT FOR CAPACITOR DISCHARGE

Analyzing this circuit, it is possible to derive the differential equation that governs the short-circuit, which is the following:

$$\frac{d^2 i_f}{dt^2} + \frac{R_{tot} + R_f}{L_{bus}} \frac{di_f}{dt} + \frac{1}{L_{bus} C_{dc}} i_f = 0$$

Where R_{tot} is the resistance including ESR of capacitor and busbar resistance, R_f is the fault resistance, C_{dc} is the capacitance of DC-bus capacitor, L_{bus} is the busbar inductance and i_f is the flowing current.

It is possible to calculate the short-circuit response by solving for the aforementioned differential equation, which depends on the aforementioned parameters, as showed in [1]. Matlab ode45 function has been used to compute the solution of this differential equation.

2.1.8 Assumptions for estimation of energy storage systems maximum short-circuit current

The following assumptions for the simulation models have been considered for the estimation of maximum short-circuit at the DC-bus:

- The battery, supercapacitor and the SMES models considered are those presented in section 2.1.1.1, section 2.2.1.1 and section 2.3.1.1

- The voltage controller is disabled.
- For the battery and supercapacitor converters, the current controller setpoint set to value in order to have nominal voltage at the DC-bus
- For SMES converter, the voltage controller setpoint set to value in order to have nominal voltage at the DC-bus
- IGBTs internal protection is activated, therefore, the fault current will flow from the ESSs to the DC-bus faulted point thought the freewheeling diode
- Snubber circuits have been neglected
- The resistance of the diodes of the IGBTs have been set to 1 mΩ
- The equivalent resistive load is set for each case at the nominal power of the ESSs converter
- Initial voltage capacitor set at the nominal voltage, which is 1100 V
- Busbar resistance is set at 1 mΩ [3]
- The fault resistance is varied from a minimum value of 1 mΩ to a maximum value of 200 mΩ [1]
- Different values of busbar loop inductance have been considered, ranging from 60 nH to 300 nH [4]-[6]
- Since the DC-bus capacitor has not been sized yet, the value of the DC-bus capacitor has been varied in a range from 1 mF to 20 mF [7]

For what concerns the analytic RLC model, the following assumptions have been considered:

- Initial voltage capacitor set at the nominal voltage
- The fault resistance is varied from a minimum value of 1 mΩ to a maximum value of 200 mΩ
- Different values of bus inductance have been considered, ranging from 60 nH to 300 nH
- Since the DC-bus capacitor has not been sized yet, the value of the DC-bus capacitor has been varied in a range from 1 mF to 20 mF

2.1.9 Assumptions for estimation of energy storage systems minimum short-circuit current

The following assumptions for the simulation models have been considered for the estimation of minimum short-circuit at the DC-bus:

- The battery supercapacitor, and SMES models considered are those presented in section 2.1.1.2, section 2.2.1.2 and section 2.3.1.2
- The voltage controller is not considered
- Current controller setpoint set to a value in order to have the lowest acceptable voltage at the DC-bus
- For SMES converter, the voltage controller setpoint set to value in order to have nominal voltage at the DC-bus
- IGBTs internal protection is activated, therefore, the fault current will flow from the ESSs to the DC-bus faulted point thought the freewheeling diode.
- Snubber circuits have been neglected

- The resistance of the diodes of the IGBTs have been set to 1 mΩ
- The equivalent resistive load is set for each case at the nominal power of the ESSs converter
- Initial voltage capacitor is set to the minimum voltage, which is 1000 V
- The fault resistance is varied from a minimum value of 1 mΩ to a maximum value of 200 mΩ
- Different values of bus inductance have been considered, ranging from 60 nH to 300 nH
- Since the DC-bus capacitor has not been sized yet, the value of the DC-bus capacitor has been varied in a range from 1 mF to 20 mF

For the analytic RLC model, the following assumptions have been considered:

- Initial voltage capacitor is set to the minimum acceptable voltage
- The fault resistance is varied from a minimum value of 1 mΩ to a maximum value of 200 mΩ
- Different values of bus inductance have been considered, ranging from 60 nH to 300 nH
- Since the DC-bus capacitor has not been sized yet, the value of the DC-bus capacitor has been varied in a range from 1 mF to 20 mF

2.2 Short-circuit results

In this section the results of the estimation of different types of short-circuit faults at the DC-bus of ESSs will be presented. A comparison between the results of simulations and the analytic method will be presented, considering various values of fault resistance, DC-bus capacitance, and inductance of the busbar. To present the results in a compact way, various tables considering variation of the key parameters will be shown, showing in particular the results of the perspective short-circuit current at 5 and 10 µs, the maximum fault-current derivative, and the let-through energy of the short-circuit. Each of these tables and plots will be presented for each ESSs in the maximum and minimum short-circuit case.

2.2.1 Results of maximum short-circuit fault at DC-bus

For the maximum short-circuit case at the DC-bus, a comparison of the analytic method and the simulation is presented in Figure 10 for the battery study case, with the DC-bus capacitor set to 10 mF, the busbar inductance set to 100 nH and the fault resistance is set to 15.8 mΩ. The analytic and simulated results match very well, confirming that the short-circuit response of the converters in completely dominated by the capacitor discharge.

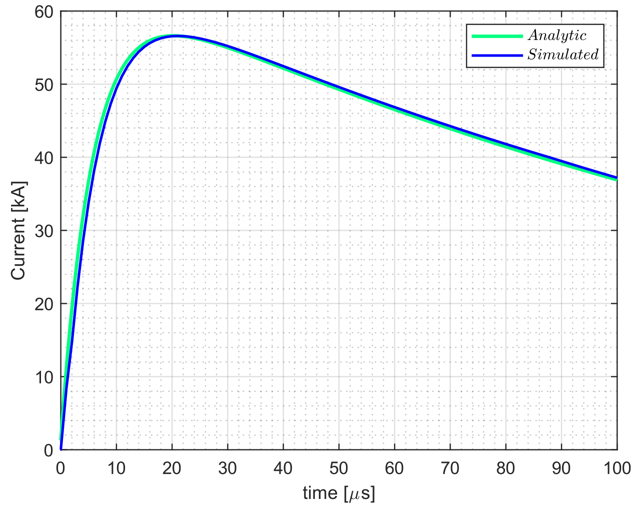

FIGURE 10: MAXIMUM SHORT-CIRCUIT – COMPARISON BETWEEN SIMULATED AND ANALYTIC METHOD

In Figure 11 , the results of maximum short-circuit for different for different values of fault resistance are presented for the battery case, with the inductance of the busbar set at 100 nH and the dc-bus capacitor set at 10 mF. It can be seen that the fault resistance impacts the maximum short-circuit current, and the current derivative. Specifically, lower values of fault resistance tend to increase the peak current and the current derivative, requiring shorter time of intervention.

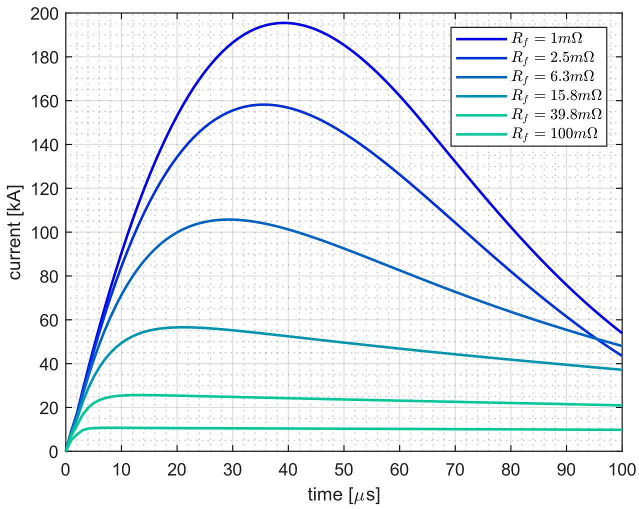

FIGURE 11: MAXIMUM SHORT-CIRCUIT RESULTS VARYING FAULT RESISTANCE – LBUS=60 nH, CDC=10 mF

In Figure 12 the results of maximum short circuit current varying the DC-bus capacitor are presented, with the value of the fault resistance set to 15.8 mΩ and the busbar inductance set to 100 nH. It can be seen that higher values of capacitance tend to increase the peak short-circuit current. However, the maximum current derivative, which occurs at the beginning of the fault event, is not influenced by the variation of the capacitance.

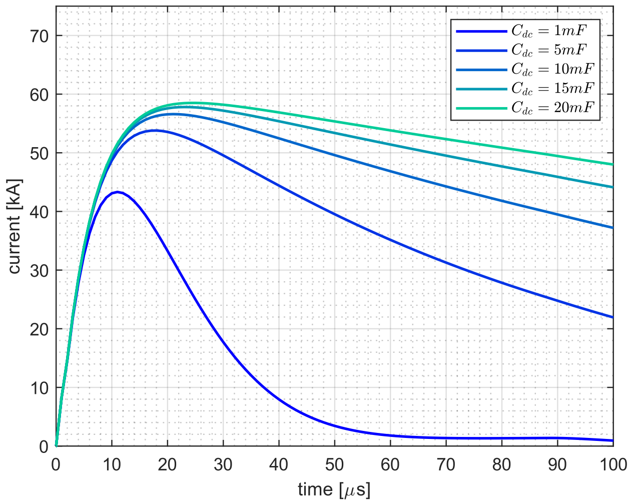

FIGURE 12. MAXIMUM SHORT-CIRCUIT RESULTS DC-BUS CAPACITOR – LBUS= nH, RF=15.8 mΩ

In Figure 13 the results of maximum short circuit current varying the busbar inductance are presented, with the value of the fault resistance set to 15.8 mΩ and the DC-bus capacitor set to 10 mF. It can be seen that lower values of busbar inductance tend to increase the current derivative, and therefore also the peak current. However, the effect on the peak current is less severe than that of the fault resistance.

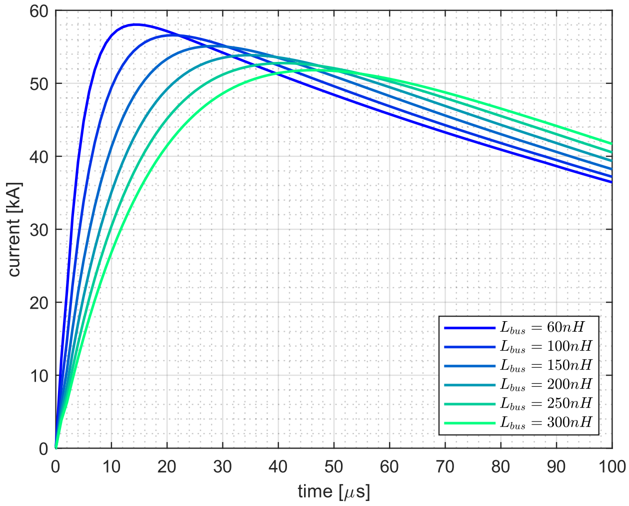

FIGURE 13: MAXIMUM SHORT-CIRCUIT RESULTS VARYING BUSBAR INDUCTANCE – CDC=10 mF, RF=15.8 mΩ

For the battery case, in Table 4 and Table 5 the results of the perspective short-circuit current at 5 µs and 10 µs respectively for different values of DC-bus capacitance and fault resistance are presented, in case where the busbar inductance values is set to 60 nH, which is the case in which the perspective short-circuit current would be higher. In Table 6 the results of the short-circuit current maximum derivative are presented, for different values of busbar inductance and fault resistance, in case where the DC-bus capacitance is set at 20 mF. Only one value of capacitance is considered because the current derivative is heavily affected by the resistance inductance of the fault path rather than the DC-bus capacitance. Lastly, the results for the let-though energy are presented in Table 7, for the case in which the busbar inductance is set to a conservative value of 60 nH.

TABLE 4: PERSPECTIVE SHORT-CIRCUIT CURRENT AT 5 μS [kA] – MAXIMUM SHORT-CIRCUIT AT DC-BUS – BATTERY CASE

Cdc [mF]	Rf [mΩ]	1.0	2.5	6.3	15.8	39.8	100
1	Analytic [kA]	70.92	67.26	59.15	44.16	25.13	11.66
	Simulated [kA]	69.77	66.01	57.83	43.07	24.76	11.59
5	Analytic [kA]	74.35	70.50	61.99	46.23	26.17	11.98
	Simulated [kA]	73.79	69.78	61.06	45.34	25.87	11.96
10	Analytic [kA]	74.79	70.91	62.35	46.49	26.30	12.02
	Simulated [kA]	74.31	70.27	61.47	45.64	26.02	12.00
15	Analytic [kA]	74.93	71.05	62.47	46.58	26.35	12.03
	Simulated [kA]	74.47	70.43	61.61	45.73	26.07	12.02
20	Analytic [kA]	75.01	71.12	62.53	46.62	26.37	12.04
	Simulated [kA]	74.56	70.51	61.68	45.78	26.09	12.03

TABLE 5: PERSPECTIVE SHORT-CIRCUIT CURRENT AT 10 μS [kA] – MAXIMUM SHORT-CIRCUIT AT DC-BUS – BATTERY CASE

Cdc [mF]	Rf [mΩ]	1.0	2.5	6.3	15.8	39.8	100
1	Analytic [kA]	106.98	96.26	75.56	46.77	23.36	11.10
	Simulated [kA]	106.28	95.59	75.06	46.62	23.32	11.06
5	Analytic [kA]	132.89	119.44	93.30	56.57	26.66	11.86
	Simulated [kA]	132.44	118.87	92.72	56.30	26.62	11.85
10	Analytic [kA]	136.36	122.54	95.68	57.88	27.09	11.96
	Simulated [kA]	135.99	122.03	95.11	57.61	27.06	11.95
15	Analytic [kA]	137.53	123.59	96.48	58.32	27.24	12.00
	Simulated [kA]	137.17	123.08	95.91	58.04	27.20	11.98
20	Analytic [kA]	138.11	124.11	96.88	58.54	27.31	12.01
	Simulated [kA]	137.77	123.62	96.31	58.26	27.28	12.00

Table 6: Maximum current derivative [kA /μs] – Maximum short-circuit at DC-bus – battery case

Lbus [nH] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
60	Analytic [kA/μs]	17.82	17.57	16.96	15.54	12.57	7.78
	Simulated [kA/μs]	14.56	14.29	13.68	12.33	9.85	6.50
100	Analytic [kA/μs]	10.80	10.70	10.45	9.86	8.54	6.05
	Simulated [kA/μs]	9.36	9.25	8.98	8.38	7.16	5.21
150	Analytic [kA/μs]	7.23	7.19	7.06	6.77	6.09	4.69
	Simulated [kA/μs]	6.70	6.65	6.51	6.18	5.49	4.27
200	Analytic [kA/μs]	5.44	5.41	5.33	5.15	4.72	3.79
	Simulated [kA/μs]	5.36	5.33	5.24	5.02	4.55	3.68
250	Analytic [kA/μs]	4.36	4.34	4.29	4.16	3.85	3.18
	Simulated [kA/μs]	4.56	4.53	4.46	4.31	3.95	3.27
300	Analytic [kA/μs]	3.64	3.62	3.58	3.49	3.26	2.74
	Simulated [kA/μs]	4.02	3.99	3.94	3.82	3.54	2.98

Table 7: Let-through energy [A^2s] with Lbus = 60 nH – Maximum short-circuit at DC-bus – battery case

Cdc [mF] \ t [us]		1	2	3	4	5	6	7	8	9	10
1	Analytic [A^2s]	130.6	904.7	2800.4	6150.9	11138.5	17799.0	26034.5	35633.8	46297.0	57664.8
	Simulated [A^2s]	103.2	566.7	1835.1	4364.7	8414.7	14099.9	21398.4	30166.6	40160.8	51062.8
5	Analytic [A^2s]	131.0	915.0	2870.6	6423.4	11911.1	19588.4	29633.3	42153.3	57191.7	74734.7
	Simulated [A^2s]	105.5	583.5	1910.9	4616.4	9082.7	15607.8	24410.1	35634.7	49359.5	65602.0
10	Analytic [A^2s]	131.1	916.3	2879.4	6458.3	12011.3	19824.0	30115.8	43045.9	58719.2	77191.6
	Simulated [A^2s]	105.8	585.7	1920.9	4649.6	9171.5	15810.3	24820.1	36392.1	50659.8	67705.4
15	Analytic [A^2s]	131.1	916.7	2882.4	6470.0	12044.8	19903.1	30278.4	43347.6	59237.1	78028.0
	Simulated [A^2s]	105.9	586.3	1923.9	4659.8	9199.5	15875.2	24953.3	36640.7	51090.5	68407.8
20	Analytic [A^2s]	131.1	916.9	2883.9	6475.8	12061.6	19942.8	30359.9	43499.1	59497.7	78449.5
	Simulated [A^2s]	105.9	586.7	1925.5	4665.4	9214.4	15909.3	25022.6	36769.3	51312.2	68768.3

Since the converter response of all the ESSs is dominated by the capacitor discharge, the results of the parametric study for the supercapacitor and SMES storage systems is very similar to the battery case. For completeness, the results are listed in the Appendix.

2.2.2 Results of minimum short-circuit fault at DC-bus

For the minimum short-circuit case at the DC-bus, a comparison of the analytic method and the simulation is presented in Figure 14 for the battery study case, with the DC-bus capacitor is set to 10 mF, the busbar inductance is set to 100 nH and the fault resistance is set to 15.8 mΩ. The results confirm the good matching between the two approaches.

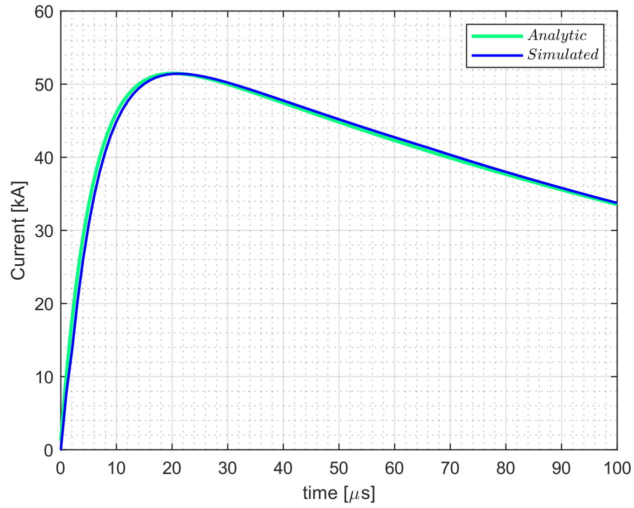

FIGURE 14: MINIMUM SHORT-CIRCUIT – COMPARISON BETWEEN SIMULATED AND ANALYTIC METHOD

In Figure 15 , the results of minimum short-circuit for different values of fault resistance are presented for the battery case, with the inductance of the busbar set at 100 nH and the DC-bus capacitor set at 10 mF. As for the maximum short-circuit case, lower values of fault resistance tend to increase the peak current and the current derivative, requiring a faster time of intervention.

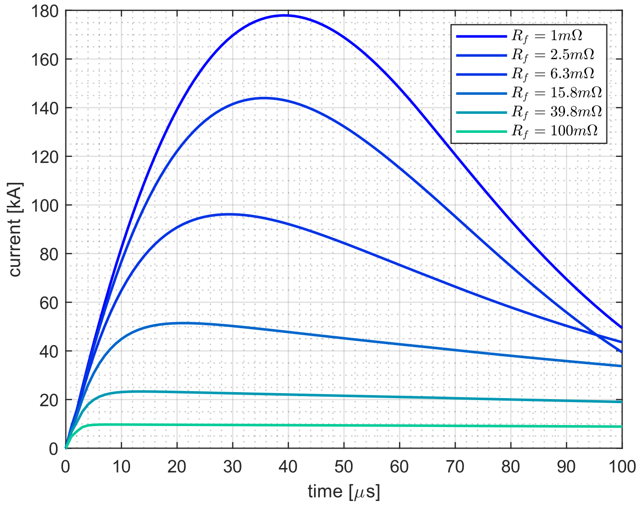

FIGURE 15 MINIMUM SHORT-CIRCUIT RESULTS VARYING FAULT RESISTANCE – LBUS=60 nH, CDC=10 mF

In Figure 16, the results of minimum short-circuit current varying the DC-bus capacitor are presented, with the value of the fault resistance set to 15.8 mΩ and the busbar inductance set to 100 nH. It can be seen that higher values of capacitance tend to increase the peak short-circuit current. However, the minimum current derivative, which occurs at the beginning of the fault event, is not influenced by the variation of the capacitance.

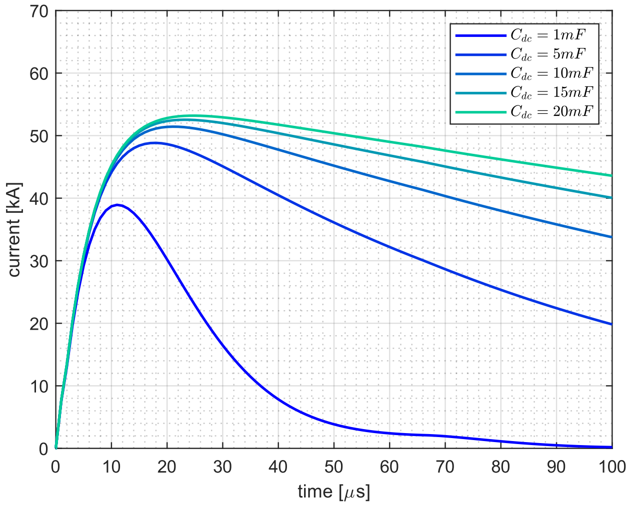

FIGURE 16: MINIMUM SHORT-CIRCUIT RESULTS DC-BUS CAPACITOR – LBUS=60 nH, RF=15.8 mΩ

In Figure 17, the results of minimum short-circuit current varying the busbar inductance are presented, with the value of the fault resistance set to 15.8 mΩ and the DC-bus capacitor set to 10 mF. It can be seen that lower values of busbar inductance tend to increase the current derivative, and therefore also the peak current. However, the effect on the peak current is less severe than that of the fault resistance.

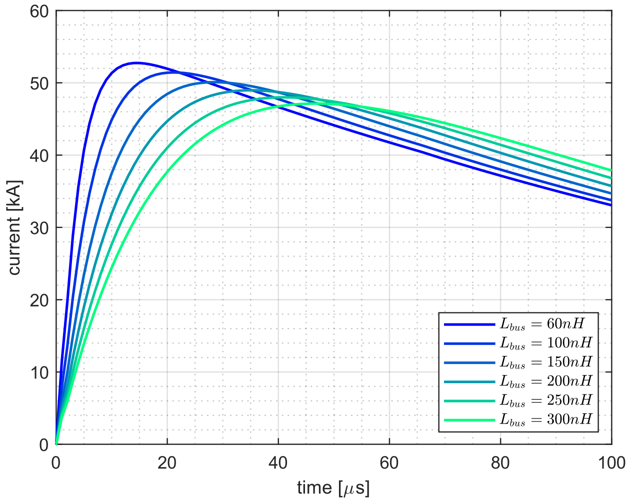

FIGURE 17: MINIMUM SHORT-CIRCUIT RESULTS VARYING BUSBAR INDUCTANCE – CDC=10 mF, RF=15.8 mΩ

The results for the battery minimum short circuit case are showed in the following tables, comparing the values obtained with both the analytic and simulated methods. Table 8 and Table 9 shows the perspective short-circuit current at 5 and 10 µs respectively, with the busbar inductance set at 60 nH. Table 10 shows the maximum current derivative for different values of fault resistance and busbar inductance. Lastly, Table 11 shows the let-trough energy until 10 µs, for different values of fault resistance and capacitance of Dc-bus capacitor.

Table 8: Perspective short-circuit current at 5 µs [kA] – Minimum short-circuit at DC-bus – Battery case

Cdc [mF] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
1	Analytic [kA]	69.50	65.42	56.55	40.71	21.86	9.43
	Simulated [kA]	72.49	67.71	57.58	40.41	21.34	9.22
5	Analytic [kA]	73.66	69.34	59.91	43.05	22.94	9.73
	Simulated [kA]	79.34	74.06	62.87	43.92	22.90	9.69
10	Analytic [kA]	74.19	69.83	60.34	43.35	23.08	9.76
	Simulated [kA]	80.25	74.90	63.57	44.38	23.11	9.75
15	Analytic [kA]	74.37	70.00	60.48	43.45	23.13	9.78
	Simulated [kA]	80.53	75.16	63.79	44.53	23.18	9.77
20	Analytic [kA]	74.46	70.08	60.55	43.50	23.15	9.78
	Simulated [kA]	80.69	75.31	63.91	44.61	23.21	9.78

Table 9: Perspective short-circuit current at 10 µs [kA] – Minimum short-circuit at DC-bus – battery case

Cdc [mF] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
1	Analytic [kA]	97.89	87.52	67.78	41.08	20.03	8.98
	Simulated [kA]	96.97	86.27	66.28	40.00	19.60	8.82
5	Analytic [kA]	124.64	111.28	85.67	50.64	23.08	9.63
	Simulated [kA]	128.28	113.78	86.56	50.54	22.98	9.60
10	Analytic [kA]	128.26	114.49	88.08	51.93	23.49	9.72
	Simulated [kA]	132.65	117.62	89.38	52.00	23.44	9.70
15	Analytic [kA]	129.47	115.57	88.90	52.36	23.62	9.75
	Simulated [kA]	134.09	118.89	90.31	52.48	23.59	9.74
20	Analytic [kA]	130.09	116.11	89.30	52.58	23.69	9.76
	Simulated [kA]	134.84	119.54	90.80	52.73	23.67	9.76

Table 10: Maximum current derivative [kA /µs] – Minimum short-circuit at DC-bus – Battery case

Lbus [nH] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
60	Analytic [kA/µs]	16.19	15.96	15.40	14.10	11.39	7.01
	Simulated [kA/µs]	13.47	13.22	12.64	11.37	9.05	5.94
100	Analytic [kA/µs]	9.81	9.72	9.50	8.96	7.75	5.48
	Simulated [kA/µs]	8.74	8.64	8.38	7.80	6.63	4.80
150	Analytic [kA/µs]	6.58	6.53	6.42	6.15	5.52	4.23
	Simulated [kA/µs]	6.33	6.28	6.14	5.82	5.14	3.97
200	Analytic [kA/µs]	4.94	4.92	4.85	4.68	4.28	3.43
	Simulated [kA/µs]	5.12	5.08	4.99	4.77	4.31	3.45
250	Analytic [kA/µs]	3.96	3.94	3.89	3.78	3.49	2.87
	Simulated [kA/µs]	4.38	4.36	4.29	4.13	3.77	3.09
300	Analytic [kA/µs]	3.30	3.29	3.25	3.16	2.95	2.47
	Simulated [kA/µs]	3.89	3.87	3.82	3.69	3.40	2.84

TABLE 11: LET-THROUGH ENERGY [A^2s] WITH LBUS = 60 NH – MINIMUM SHORT-CIRCUIT AT DC-BUS – BATTERY CASE

Cdc [mF] \ t [us]		1	2	3	4	5	6	7	8	9	10
1	Analytic [A^2s]	109.1	751.6	2322.4	5096.3	9223.5	14733.2	21544.1	29481.2	38296.7	47693.2
	Simulated [A^2s]	85.5	464.9	1494.0	3539.2	6808.7	11395.6	17283.7	24359.4	32428.8	41237.7
5	Analytic [A^2s]	109.4	760.2	2380.7	5322.5	9864.2	16216.2	24525.3	34880.2	47316.5	61822.5
	Simulated [A^2s]	89.8	491.5	1596.8	3840.7	7537.1	12930.7	20201.0	29467.2	40793.6	54194.6
10	Analytic [A^2s]	109.4	761.2	2388.1	5351.4	9947.3	16411.4	24925.1	35619.5	48581.2	63856.4
	Simulated [A^2s]	90.4	495.1	1610.8	3881.6	7636.5	13142.0	20607.5	30190.1	42000.1	56105.2
15	Analytic [A^2s]	109.5	761.6	2390.6	5361.1	9975.1	16477.0	25059.7	35869.3	49010.0	64548.8
	Simulated [A^2s]	90.6	496.0	1614.6	3893.4	7666.1	13206.6	20734.3	30419.7	42388.9	56728.5
20	Analytic [A^2s]	109.5	761.8	2391.8	5366.0	9989.0	16509.9	25127.3	35994.8	49225.8	64897.7
	Simulated [A^2s]	90.7	496.7	1617.1	3900.6	7683.5	13243.5	20805.2	30545.7	42599.3	57062.2

As for the maximum short-circuit case, since the converter response of all the ESSs is dominated by the capacitor discharge, the results of the parametric study for the supercapacitor and SMES storage systems is very similar to the battery case. For completeness, the results are listed in the Appendix.

3 Appendix

3.1 Simulation results for supercapacitor

3.1.1 Maximum short-circuit

TABLE 12: PERSPECTIVE SHORT-CIRCUIT CURRENT AT 5 µS [KA] – MAXIMUM SHORT-CIRCUIT AT DC-BUS – SUPERCAPACITOR CASE

Cdc [mF] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
1	Analytic [kA]	75.88	71.46	61.85	44.64	24.04	10.38
	Simulated [kA]	72.61	68.56	59.69	43.64	23.93	10.39
5	Analytic [kA]	80.33	75.65	65.45	47.16	25.22	10.70
	Simulated [kA]	76.67	72.38	62.98	45.96	25.04	10.70
10	Analytic [kA]	80.90	76.19	65.91	47.48	25.37	10.74
	Simulated [kA]	77.19	72.87	63.40	46.26	25.19	10.75
15	Analytic [kA]	81.09	76.36	66.07	47.59	25.42	10.76
	Simulated [kA]	77.36	73.02	63.54	46.35	25.23	10.76
20	Analytic [kA]	81.18	76.45	66.14	47.65	25.44	10.76
	Simulated [kA]	77.46	73.12	63.62	46.41	25.26	10.77

Table 13: Perspective short-circuit current at 10 µs [kA] – Maximum short-circuit at DC-bus – Supercapacitor case

Cdc [mF] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
1	Analytic [kA]	107.59	96.25	74.60	45.26	22.06	9.88
	Simulated [kA]	106.90	95.85	74.66	45.57	22.18	9.90
5	Analytic [kA]	136.65	122.06	94.06	55.68	25.39	10.60
	Simulated [kA]	134.25	120.20	93.09	55.54	25.42	10.60
10	Analytic [kA]	140.57	125.54	96.69	57.08	25.84	10.69
	Simulated [kA]	137.94	123.48	95.57	56.88	25.85	10.70
15	Analytic [kA]	141.89	126.72	97.57	57.55	25.99	10.72
	Simulated [kA]	139.17	124.57	96.40	57.32	26.00	10.73
20	Analytic [kA]	142.55	127.30	98.01	57.79	26.06	10.74
	Simulated [kA]	139.82	125.15	96.84	57.56	26.08	10.74

Table 14: Maximum current derivative [kA /µs] – Maximum short-circuit at DC-bus – Supercapacitor case

Lbus [nH] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
60	Analytic [kA/µs]	17.86	17.63	17.07	15.75	13.00	8.47
	Simulated [kA/µs]	13.68	13.50	13.08	12.12	10.16	7.07
100	Analytic [kA/µs]	10.82	10.74	10.52	10.00	8.84	6.61
	Simulated [kA/µs]	8.39	8.33	8.16	7.78	6.93	5.39
150	Analytic [kA/µs]	7.25	7.21	7.11	6.86	6.29	5.10
	Simulated [kA/µs]	5.71	5.68	5.60	5.42	4.99	4.15
200	Analytic [kA/µs]	5.45	5.43	5.37	5.22	4.88	4.13
	Simulated [kA/µs]	4.36	4.34	4.30	4.19	3.93	3.39
250	Analytic [kA/µs]	4.37	4.35	4.31	4.22	3.98	3.46
	Simulated [kA/µs]	3.55	3.53	3.50	3.43	3.25	2.87
300	Analytic [kA/µs]	3.64	3.63	3.60	3.53	3.36	2.98
	Simulated [kA/µs]	3.00	2.99	2.97	2.92	2.79	2.50

TABLE 15: LET-THROUGH ENERGY [A^2s] WITH LBUS = 60 nH – MAXIMUM SHORT-CIRCUIT AT DC-BUS – SUPERCAPACITOR CASE

Cdc [mF] \ t [us]		1	2	3	4	5	6	7	8	9	10
1	Analytic [A^2s]	113.3	842.4	2672.3	5943.7	10846.4	17423.6	25583.5	35119.9	45737.1	57077.7
	Simulated [A^2s]	92.3	649.6	2176.6	5049.3	9496.2	15599.4	23303.8	32435.8	42725.5	53834.9
5	Analytic [A^2s]	113.6	851.5	2737.1	6200.8	11584.3	19146.4	29068.8	41462.5	56373.8	73791.7
	Simulated [A^2s]	93.3	661.7	2243.8	5293.7	10176.1	17171.5	26481.6	38236.1	52498.3	69272.3
10	Analytic [A^2s]	113.6	852.6	2745.4	6233.7	11679.8	19373.0	29535.7	42330.0	57863.3	76194.1
	Simulated [A^2s]	93.4	663.3	2252.4	5325.1	10264.6	17379.1	26908.6	39030.9	53867.9	71490.8
15	Analytic [A^2s]	113.6	853.0	2748.1	6244.7	11711.9	19449.1	29692.9	42623.0	58368.2	77011.7
	Simulated [A^2s]	93.5	663.6	2254.8	5334.6	10292.2	17445.3	27046.8	39291.4	54321.1	72231.1
20	Analytic [A^2s]	113.7	853.2	2749.5	6250.2	11727.9	19487.3	29771.8	42770.3	58622.3	77423.7
	Simulated [A^2s]	93.5	664.2	2257.2	5342.2	10311.6	17487.9	27130.8	39443.5	54578.4	72642.9

3.1.2 Minimum short-circuit

TABLE 16: PERSPECTIVE SHORT-CIRCUIT CURRENT AT 50 μS [kA] – MINIMUM SHORT-CIRCUIT AT DC-BUS – SUPERCAPACITOR CASE

Cdc [mF] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
1	Analytic [kA]	69.50	65.42	56.55	40.71	21.86	9.43
	Simulated [kA]	65.83	62.15	54.09	39.54	21.68	9.41
5	Analytic [kA]	73.66	69.34	59.91	43.05	22.94	9.73
	Simulated [kA]	69.60	65.70	57.16	41.70	22.72	9.71
10	Analytic [kA]	74.19	69.83	60.34	43.35	23.08	9.76
	Simulated [kA]	70.09	66.15	57.55	41.98	22.85	9.75
15	Analytic [kA]	74.37	70.00	60.48	43.45	23.13	9.78
	Simulated [kA]	70.25	66.31	57.68	42.07	22.89	9.76
20	Analytic [kA]	74.46	70.08	60.55	43.50	23.15	9.78
	Simulated [kA]	70.33	66.38	57.74	42.11	22.91	9.77

TABLE 17: PERSPECTIVE SHORT-CIRCUIT CURRENT AT 10 μS [kA] – MINIMUM SHORT-CIRCUIT AT DC-BUS – SUPERCAPACITOR CASE

Cdc [mF] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
1	Analytic [kA]	97.89	87.52	67.78	41.08	20.03	8.98
	Simulated [kA]	96.92	86.89	67.68	41.31	20.10	8.97
5	Analytic [kA]	124.64	111.28	85.67	50.64	23.08	9.63
	Simulated [kA]	121.84	109.87	84.46	50.39	23.07	9.62
10	Analytic [kA]	128.26	114.49	88.08	51.93	23.49	9.72
	Simulated [kA]	125.21	112.07	86.73	51.61	23.46	9.71
15	Analytic [kA]	129.47	115.57	88.90	52.36	23.62	9.75
	Simulated [kA]	126.34	113.08	87.49	52.02	23.59	9.73
20	Analytic [kA]	130.09	116.11	89.30	52.58	23.69	9.76
	Simulated [kA]	126.90	113.58	87.87	52.23	23.66	9.75

TABLE 18: MAXIMUM CURRENT DERIVATIVE [kA /µs] – MINIMUM SHORT-CIRCUIT AT DC-BUS – SUPERCAPACITOR CASE

Lbus [nH] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
60	Analytic [kA/µs]	16.19	15.96	15.40	14.10	11.39	7.01
	Simulated [kA/µs]	12.46	12.30	11.91	11.03	9.24	6.42
100	Analytic [kA/µs]	9.81	9.72	9.50	8.96	7.75	5.48
	Simulated [kA/µs]	7.67	7.60	7.45	7.10	6.32	4.90
150	Analytic [kA/µs]	6.58	6.53	6.42	6.15	5.52	4.23
	Simulated [kA/µs]	5.23	5.20	5.13	4.96	4.56	3.78
200	Analytic [kA/µs]	4.94	4.92	4.85	4.68	4.28	3.43
	Simulated [kA/µs]	4.01	3.99	3.95	3.84	3.60	3.09
250	Analytic [kA/µs]	3.96	3.94	3.89	3.78	3.49	2.87
	Simulated [kA/µs]	3.27	3.26	3.23	3.16	2.99	2.63
300	Analytic [kA/µs]	3.30	3.29	3.25	3.16	2.95	2.47
	Simulated [kA/µs]	2.78	2.77	2.75	2.69	2.57	2.30

TABLE 19: LET-THROUGH ENERGY [A^2s] WITH LBUS = 60 nH – MINIMUM SHORT-CIRCUIT AT DC-BUS – SUPERCAPACITOR CASE

Cdc [mF] \ t [us]		1	2	3	4	5	6	7	8	9	10
1	Analytic [A^2s]	109.1	751.6	2322.4	5096.3	9223.5	14733.2	21544.1	29481.2	38296.7	47693.2
	Simulated [A^2s]	76.4	535.6	1791.9	4153.9	7809.1	12824.8	19156.2	26660.6	35116.9	44247.5
5	Analytic [A^2s]	109.4	760.2	2380.7	5322.5	9864.2	16216.2	24525.3	34880.2	47316.5	61822.5
	Simulated [A^2s]	77.4	547.2	1852.5	4367.0	8390.9	14154.7	21824.6	31507.1	43254.4	57069.8
10	Analytic [A^2s]	109.4	761.2	2388.1	5351.4	9947.3	16411.4	24925.1	35619.5	48581.2	63856.4
	Simulated [A^2s]	77.6	548.7	1860.3	4394.8	8467.4	14331.6	22185.2	32174.4	44399.6	58919.3
15	Analytic [A^2s]	109.5	761.6	2390.6	5361.1	9975.1	16477.0	25059.7	35869.3	49010.0	64548.8
	Simulated [A^2s]	77.6	549.2	1862.9	4404.1	8492.9	14390.8	22306.3	32399.4	44787.1	59547.7
20	Analytic [A^2s]	109.5	761.8	2391.8	5366.0	9989.0	16509.9	25127.3	35994.8	49225.8	64897.7
	Simulated [A^2s]	77.6	549.3	1864.0	4408.0	8504.4	14418.4	22363.8	32507.7	44975.6	59855.7

3.2 SMES

3.2.1 Maximum short-circuit

TABLE 20: PERSPECTIVE SHORT-CIRCUIT CURRENT AT 5 μS [kA] – MAXIMUM SHORT-CIRCUIT AT DC-BUS – SMESS CASE

Cdc [mF] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
1	Analytic [kA]	72.46	68.48	59.73	43.77	24.01	10.41
	Simulated [kA]	69.25	65.53	57.38	42.54	23.88	10.44
5	Analytic [kA]	76.20	72.01	62.79	45.96	25.06	10.71
	Simulated [kA]	72.75	68.82	60.20	44.51	24.80	10.70
10	Analytic [kA]	76.68	72.46	63.18	46.24	25.20	10.74
	Simulated [kA]	73.19	69.23	60.55	44.75	24.92	10.73
15	Analytic [kA]	76.84	72.61	63.31	46.33	25.24	10.76
	Simulated [kA]	73.34	69.37	60.67	44.83	24.96	10.74
20	Analytic [kA]	76.92	72.68	63.38	46.38	25.26	10.76
	Simulated [kA]	73.43	69.45	60.74	44.89	24.98	10.75

TABLE 21: PERSPECTIVE SHORT-CIRCUIT CURRENT AT 10 μS [kA] – MAXIMUM SHORT-CIRCUIT AT DC-BUS – SMESS CASE

Cdc [mF] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
1	Analytic [kA]	107.05	96.02	74.84	45.67	22.21	9.91
	Simulated [kA]	106.08	95.39	74.75	45.99	22.38	9.95
5	Analytic [kA]	133.92	119.98	93.03	55.55	25.43	10.60
	Simulated [kA]	131.47	118.00	91.90	55.31	25.42	10.60
10	Analytic [kA]	137.53	123.20	95.47	56.87	25.85	10.69
	Simulated [kA]	134.86	121.02	94.18	56.55	25.82	10.68
15	Analytic [kA]	138.74	124.28	96.30	57.32	25.99	10.72
	Simulated [kA]	136.01	122.04	94.96	56.97	25.96	10.71
20	Analytic [kA]	139.35	124.82	96.71	57.54	26.06	10.74
	Simulated [kA]	136.62	122.58	95.37	57.19	26.03	10.72

TABLE 22: MAXIMUM CURRENT DERIVATIVE [kA /μS] – MAXIMUM SHORT-CIRCUIT AT DC-BUS – SMESS CASE

Lbus [nH] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
60	Analytic [kA/μs]	17.86	17.63	17.07	15.75	13.00	8.47
	Simulated [kA/μs]	13.46	13.24	12.71	11.56	9.38	6.31
100	Analytic [kA/μs]	10.82	10.74	10.52	10.00	8.84	6.61
	Simulated [kA/μs]	8.25	8.17	7.97	7.50	6.52	4.89
150	Analytic [kA/μs]	7.25	7.21	7.11	6.86	6.29	5.10
	Simulated [kA/μs]	5.60	5.56	5.47	5.24	4.75	3.83
200	Analytic [kA/μs]	5.45	5.43	5.37	5.22	4.88	4.13
	Simulated [kA/μs]	4.26	4.24	4.18	4.05	3.75	3.15
250	Analytic [kA/μs]	4.37	4.35	4.31	4.22	3.98	3.46
	Simulated [kA/μs]	3.45	3.43	3.40	3.31	3.11	2.69
300	Analytic [kA/μs]	3.64	3.63	3.60	3.53	3.36	2.98
	Simulated [kA/μs]	2.91	2.90	2.87	2.81	2.66	2.35

Table 23: Let-through energy [A^2s] with Lbus = 60 nH – Maximum short-circuit at DC-bus – SMESS case

Cdc [mF] \ t [us]		1	2	3	4	5	6	7	8	9	10
1	Analytic [A^2s]	113.3	842.4	2672.3	5943.7	10846.4	17423.6	25583.5	35119.9	45737.1	57077.7
	Simulated [A^2s]	89.6	516.9	1732.8	4200.3	8187.2	13814.5	21063.9	29793.5	39759.4	50641.8
5	Analytic [A^2s]	113.6	851.5	2737.1	6200.8	11584.3	19146.4	29068.8	41462.5	56373.8	73791.7
	Simulated [A^2s]	90.4	525.2	1780.7	4384.9	8724.4	15100.6	23735.0	34775.4	48302.3	64335.2
10	Analytic [A^2s]	113.6	852.6	2745.4	6233.7	11679.8	19373.0	29535.7	42330.0	57863.3	76194.1
	Simulated [A^2s]	90.5	526.0	1786.2	4407.1	8791.3	15264.9	24084.6	35443.6	49477.5	66270.4
15	Analytic [A^2s]	113.6	853.0	2748.1	6244.7	11711.9	19449.1	29692.9	42623.0	58368.2	77011.7
	Simulated [A^2s]	90.5	526.4	1788.2	4415.2	8814.9	15322.2	24205.6	35673.9	49882.2	66937.2
20	Analytic [A^2s]	113.7	853.2	2749.5	6250.2	11727.9	19487.3	29771.8	42770.3	58622.3	77423.7
	Simulated [A^2s]	90.5	526.8	1790.0	4421.1	8830.5	15357.4	24276.6	35804.9	50107.1	67301.8

3.2.2 Minimum short-circuit

Table 24: Perspective short-circuit current at 5 μs [kA] – Minimum short-circuit at DC-bus – SMES case

Cdc [mF] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
1	Analytic [kA]	66.42	62.74	54.65	39.94	21.84	9.46
	Simulated [kA]	62.60	59.10	51.49	37.88	21.17	9.30
5	Analytic [kA]	69.93	66.04	57.51	41.98	22.81	9.73
	Simulated [kA]	67.02	63.24	55.04	40.36	22.39	9.70
10	Analytic [kA]	70.37	66.46	57.88	42.24	22.94	9.77
	Simulated [kA]	67.61	63.79	55.50	40.69	22.55	9.75
15	Analytic [kA]	70.52	66.60	58.00	42.33	22.98	9.78
	Simulated [kA]	67.79	63.96	55.65	40.79	22.60	9.77
20	Analytic [kA]	70.60	66.67	58.06	42.37	23.00	9.78
	Simulated [kA]	67.89	64.05	55.73	40.84	22.63	9.78

Table 25: Perspective short-circuit current at 10 μs [kA] – Minimum short-circuit at DC-bus – SMES case

Cdc [mF] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
1	Analytic [kA]	97.42	87.34	68.01	41.46	20.17	9.01
	Simulated [kA]	95.44	85.67	66.95	41.14	20.04	8.90
5	Analytic [kA]	122.18	109.41	84.74	50.52	23.11	9.64
	Simulated [kA]	120.15	107.61	83.51	50.13	23.07	9.62
10	Analytic [kA]	125.51	112.37	86.99	51.74	23.50	9.72
	Simulated [kA]	123.55	110.63	85.78	51.36	23.48	9.71
15	Analytic [kA]	126.63	113.37	87.75	52.15	23.63	9.75
	Simulated [kA]	124.67	111.62	86.53	51.76	23.61	9.74
20	Analytic [kA]	127.19	113.87	88.13	52.35	23.69	9.76
	Simulated [kA]	125.25	112.14	86.92	51.97	23.68	9.76

Table 26: Maximum current derivative [kA/μs] – Minimum short-circuit at DC-bus – SMES case

Lbus [nH] \ Rf [mΩ]		1.0	2.5	6.3	15.8	39.8	100
60	Analytic [kA/μs]	16.19	15.96	15.40	14.10	11.39	7.01
	Simulated [kA/μs]	13.47	13.22	12.64	11.37	9.05	5.94
100	Analytic [kA/μs]	9.81	9.72	9.50	8.96	7.75	5.48
	Simulated [kA/μs]	8.74	8.64	8.38	7.80	6.63	4.80
150	Analytic [kA/μs]	6.58	6.53	6.42	6.15	5.52	4.23
	Simulated [kA/μs]	6.33	6.28	6.14	5.82	5.14	3.97
200	Analytic [kA/μs]	4.94	4.92	4.85	4.68	4.28	3.43
	Simulated [kA/μs]	5.12	5.08	4.99	4.77	4.31	3.45
250	Analytic [kA/μs]	3.96	3.94	3.89	3.78	3.49	2.87
	Simulated [kA/μs]	4.38	4.36	4.29	4.13	3.77	3.09
300	Analytic [kA/μs]	3.30	3.29	3.25	3.16	2.95	2.47
	Simulated [kA/μs]	3.89	3.87	3.82	3.69	3.40	2.84

Table 27: Let-through energy [A^2s] with Lbus = 60 nH – Minimum short-circuit at DC-bus – SMES case

Cdc [mF] \ t [us]		1	2	3	4	5	6	7	8	9	10
1	Analytic [A^2s]	109.1	751.6	2322.4	5096.3	9223.5	14733.2	21544.1	29481.2	38296.7	47693.2
	Simulated [A^2s]	85.5	464.9	1494.0	3539.2	6808.7	11395.6	17283.7	24359.4	32428.8	41237.7
5	Analytic [A^2s]	109.4	760.2	2380.7	5322.5	9864.2	16216.2	24525.3	34880.2	47316.5	61822.5
	Simulated [A^2s]	89.8	491.5	1596.8	3840.7	7537.1	12930.7	20201.0	29467.2	40793.6	54194.6
10	Analytic [A^2s]	109.4	761.2	2388.1	5351.4	9947.3	16411.4	24925.1	35619.5	48581.2	63856.4
	Simulated [A^2s]	90.4	495.1	1610.8	3881.6	7636.5	13142.0	20607.5	30190.1	42000.1	56105.2
15	Analytic [A^2s]	109.5	761.6	2390.6	5361.1	9975.1	16477.0	25059.7	35869.3	49010.0	64548.8
	Simulated [A^2s]	90.6	496.0	1614.6	3893.4	7666.1	13206.6	20734.3	30419.7	42388.9	56728.5
20	Analytic [A^2s]	109.5	761.8	2391.8	5366.0	9989.0	16509.9	25127.3	35994.8	49225.8	64897.7
	Simulated [A^2s]	90.7	496.7	1617.1	3900.6	7683.5	13243.5	20805.2	30545.7	42599.3	57062.2

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